A MINIATURE 2-18 GHz MONOLITHIC GaAs DISTRIBUTED AMPLIFIER*

Wayne Kennan, Tom Andrade, Charlie Huang

Avantek, Inc., Santa Clara, California

ABSTRACT

A 2-18 GHz monolithic GaAs distributed amplifier has been developed with over 6 dB gain ± 0.5 dB gain ripple, less than 2.0 input and output VSWR, less than 7.5 dB noise figure, and greater than 17 dBm power output capability. The amplifier is designed with dual-gate GaAs FET's and measures .75 mm by .85 mm (.64 mm^2). The small size insures high circuit yield and makes the part cost effective for general applications.

INTRODUCTION

Distributed amplification has joined the ranks of reactive and feedback matching as a viable approach to GaAs FET amplifier design[1,2,3]. Although it typically cannot meet the power or noise performance[4] of narrow band reactively matched amplifiers, the distributed amplifier is an excellent candidate for general purpose gain blocks as it offers wide bandwidth and low VSWR, while maintaining respectable noise and power performance. In this design, dual-gate FET's are used in place of the traditional single-gate FET's as the active elements. The inherently high output impedance and isolation of dual-gate FET's offer many advantages to distributed amplifiers in terms of gain-bandwidth product, gain flatness, output VSWR, and isolation. In addition, control of the gate 2 voltage makes this amplifier useful for many wideband control functions such as limiting, AGC, and switching. This paper will describe the design, fabrication, and performance of the distributed amplifier.

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CIRCUIT DESIGN

The topology of the amplifier is shown in Figure 1. There are four dual-gate FET's with a total gate width of 825 microns. Unlike other distributed amplifier designs, the individual FET gate widths vary in size from 175 microns to 225 microns. This degree of freedom is not available to hybrid MIC designers and is used in this case to absorb the parasitic input and output pad capacitances of the chip. The resulting VSWR is much lower than an equivalent 825 micron design using identical FET's.

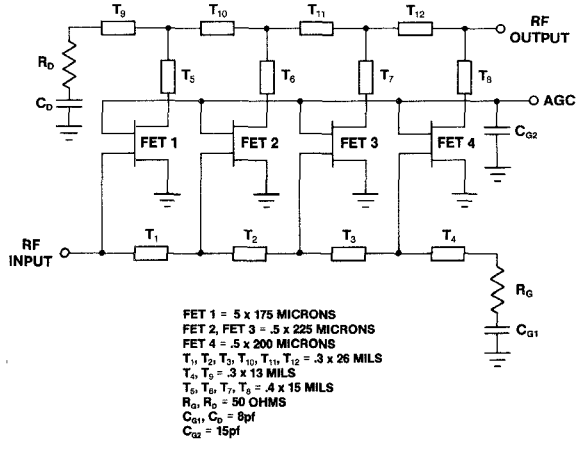

Figure 1. Schematic Diagram of the Distributed Amplifier

The second gates of all the FET's are connected together and RF bypassed to ground. This insures cascode operation of the FET's and provides RF isolation from the AGC bias circuitry. The FET sources are shorted directly to ground thus requiring both positive (drain) and negative (gate) bias supplies. In order to conserve chip area and provide maximum flexibility to the user, the bias circuitry was not included in the design. Instead, bias chokes and/or resistors must be provided off-chip.

Another feature of the design is the lack of input and output transmission line sections which are normally half the length of the sections between the FET's. These elements are absorbed into the input and output bond wires which have approximately 0.3 nH of inductance. This feature saves chip area and permits standard chip mounting techniques to be used without degradation to VSWR or gain. Series transmission lines are connected to the FET drains in order to equalize phase velocities of the incoming and outgoing signals. This can also be achieved with shunt drain capacitors but the transmission lines are more reproducible and are useful for maintaining flat gain at the high end of the frequency range.

The simulated gain and isolation of the chip are plotted in Figure 2. From 2-18 GHz, the predicted gain is 7.25 dB ± 0.22 dB with greater than 35 dB isolation. Predicted return loss is shown in Figure 3 and is greater than 14 dB (1.5 VSWR) at both the input and output. This performance translates into very high stability (K factor greater than 15) and excellent cascadability.

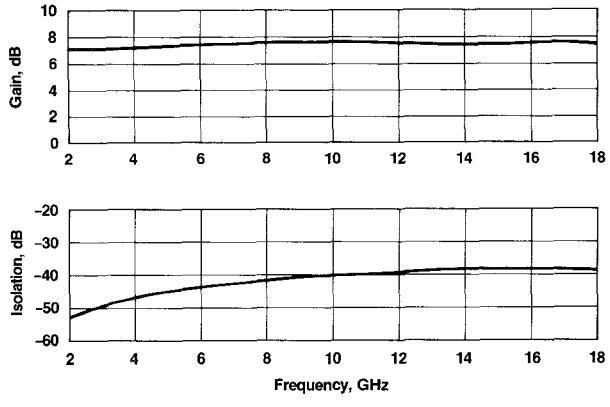

Figure 2. Predicted Gain and Isolation of the Distributed Amplifier

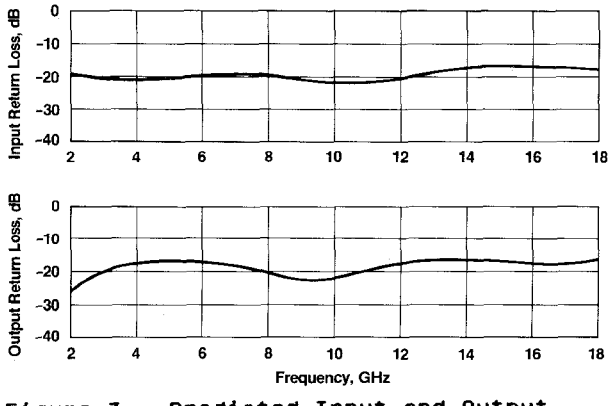

Figure 3. Predicted Input and Output Return Loss of the Distributed Amplifier

CIRCUIT FABRICATION

The IC process used to fabricate the distributed amplifier is identical to that used for previous designs[5]. The fabrication process is based on ion-implanted GaAs active layers which form both the active area of the FET and resistors. The FET gates are 0.5 micron long and are fabricated with a TiW/Au refractory metal system which is plated in a manner that combines small gate length with large gate area cross section.[6] The dual gate FET's used in this design were adapted from discrete dual gate FET's which were carefully modelled.[7] A photograph of the amplifier is shown in Figure 4.

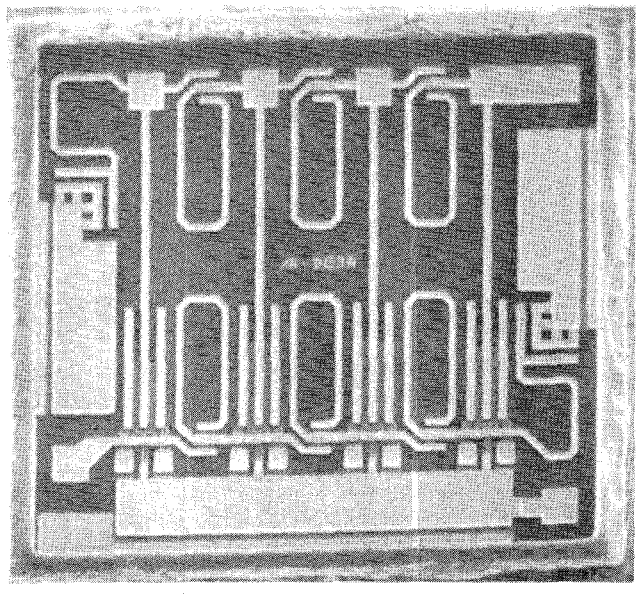

Figure 4. SEM Micrograph of the Distributed Amplifier

Miniaturization of the amplifier was accomplished in two ways. First, the inductors between the FET's are wound one turn to make them area efficient. These one turn inductors are easily modeled and realized with lines 8 microns wide and 2.5 microns thick to maintain both high impedance and reliable current carrying capability. The second contribution to miniaturization is the wraparound ground which provides access to ground along the entire perimeter of the chip. This results in extremely low parasitic inductance and excellent reproducibility in a very small area. A comparable design using via hole grounds would have degraded performance at 18 GHz and require significantly larger chip area.

CIRCUIT PERFORMANCE

After fabrication the wafers are DC probed for saturated current, transconductance, and pinch-off voltage. The chips are then separated and visually inspected. Selected IC's that pass both DC and visual tests are mounted on 15 mil thick alumina substrates for evaluation. Exclusive of bias circuitry, the entire 2-18 GHz amplifier consists of one substrate, one IC and two bond wires. Bias is normally injected through bias tees but may also be injected through additional bond wires and resistors. The data presented in this paper was measured on IC's mounted on this substrate without any tuning. Substrate loss and VSWR degradation are not subtracted from the results.

Figure 5 shows gain and isolation measured on a typical amplifier fabricated within process specifications. The gain achieved is 6.3 dB ± 0.5 dB with greater than 25 dB isolation. Figure 6 shows input and output return loss for the same chip. The worst case VSWR is 2.0 although it is less than 1.5 over most of the band. In this case, the device is biased at 4.0 volts V_{DS} and 80 mA I_{DS} which is approximately half the saturated current level. Higher levels of gain are achieved with higher drain current but gain flatness does degrade slightly.

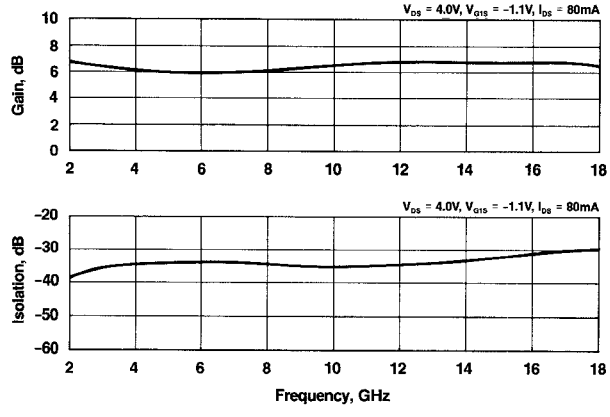

Figure 5. Measured Gain and Isolation of a Typical Distributed Amplifier

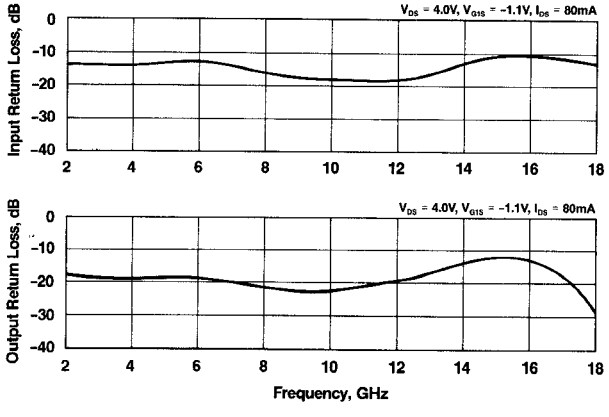

Figure 6. Measured Input and Output Return Loss of a Typical Distributed Amplifier

Noise and power performance of the chip are shown in Figure 7. The noise figure is typically less than 6 dB although it rises to 7.5 dB at 18 GHz. This can be reduced to 7.0 dB by adjusting the bias but with a corresponding 1.0 dB loss in associated gain. Output power capability is shown in the lower graph with the IC biased at 6 volts and 120 mA. The output power is plotted from 2-18 GHz with constant input power levels of 10 dBm and 15 dBm. The device is capable of 20 dBm output power over most of the band but degrades to 17 dBm at 18 GHz. Gain compression is obviously more severe at the higher frequencies as can be seen from the two plots.

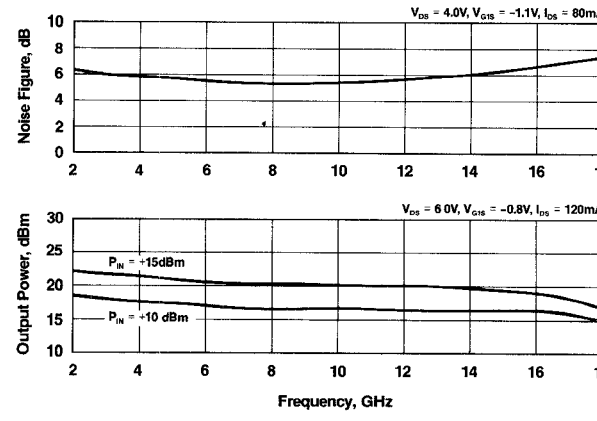

Figure 7. Measured Noise Figure and Output Power of a Typical Distributed Amplifier

The last figure, Figure 8, illustrates a number of the applications for which this IC may be useful. For AGC use the gain variation is very flat over the full 2-18 GHz range when the gate 2 voltage is varied between 0 volts and -1 volt as shown. This property may be useful for temperature compensation of the amplifier. When the gate 2 voltage is made increasingly negative, the device becomes lossy and may be used for limiting applications. Finally, when the voltage is increased to -4 volts, the drain current drops to nearly 0 mA and the device provides over 25 dB isolation. This property could be easily exploited for switching since VSWR and reverse isolation remain less than 2:1 and greater than 25 dB, respectively, under all bias conditions.

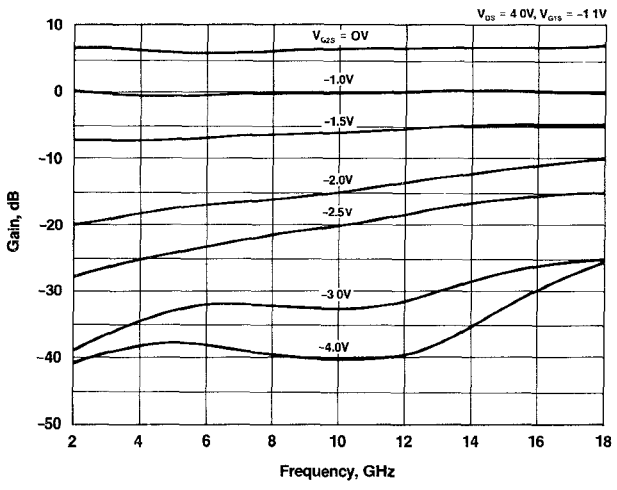

Figure 8. Measured Gain/Loss as a Function of Gate 2 Voltage

CONCLUSION

A very small 2-18 GHz monolithic GaAs distributed amplifier with over 6 dB gain has been described. Based on chip size, performance, and application flexibility the device is very attractive for many wideband as well as narrowband uses.

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